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3D Full Wave EM Modeling of IC Packages
A New Approach

Dan Lambalot, Director Of Engineering, Socionext America Inc
Jason Chan, Cadence Design Systems

Agenda

- Intro to Socionext America
- Review Test Case
- Pros & Cons of Traditional High-Speed IO Modeling Flow using Model Segmentation Approach
  - Computational Design Flow
- Introduction to Clarity 3D Solver
- Streamlined Approach: No Model Segmentation Necessary
  - Accelerated Computational Prototyping Flow
- Comparison of Approaches

Author Overview

About Socionext America

Bayside Design Inc. (BDI) was founded in 2002 to provide the most comprehensive high speed engineering design services with primary focus on High Speed Package and Board Design Services and Solutions. Majority of the customers served by BDI are leading IP providers, high end technology companies in Compute, Storage, Communication, RF, Microwave, Millimeterwave, Optical and Consumer markets. Bayside Design was acquired by Socionext in January, 2016 and is now doing business as Socionext America.

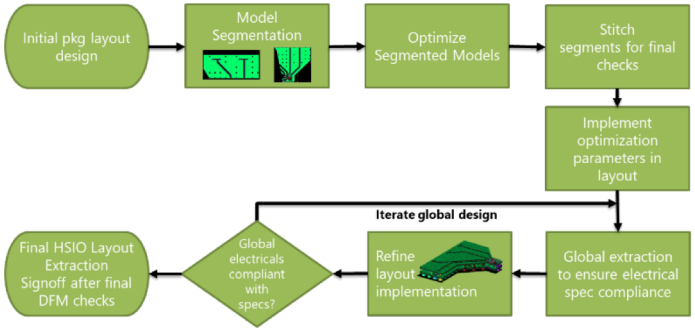
About the Authors

Daniel Lambalot is Director of Engineering of Socionext. Daniel joined Socionext through the acquisition of Bayside Design, a premier design services company with expertise in high-performance signal- and power-integrity for IC packaging and boards. Prior to Bayside Design, he worked at Velio Communications, Compaq, and Digital Equipment Corp. Daniel earned his BSEE from Northeastern University and MSEE from the University of Illinois at Urbana Champaign.

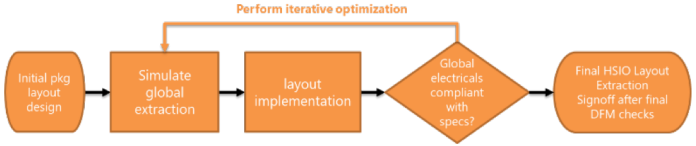
Jason Chan received his MSEE degree in Applied Electromagnetics from the University of New Hampshire. He is currently working as a Senior Principal Product Engineer for Cadence Design Systems where his primary responsibilities reside in customer engagement & product engineering support for the Sigrity 3D Field Solver platform. Prior to joining Cadence, he previously served at Invecas, Altera, LSI, Huawei Technologies, Samtec and Amphenol-TCS. His professional interests reside in high speed system-level architectural design/simulation and applied electrodynamics.

Abstract

- Traditional 3D field solver methodologies are capable of producing accurate results
- Traditional methodology requires that one must carefully truncate the problem space by slicing up the model into smaller segments to fit within local computing resources
- New methodology, enabled by new Cadence technology, will demonstrate that larger models can be created faster while maintaining gold-standard accuracy
- Test case will be reviewed using both flows and the performance results will be presented



Traditional 3D Expert Flow



A new flow enabled with New technology that requires less expertise

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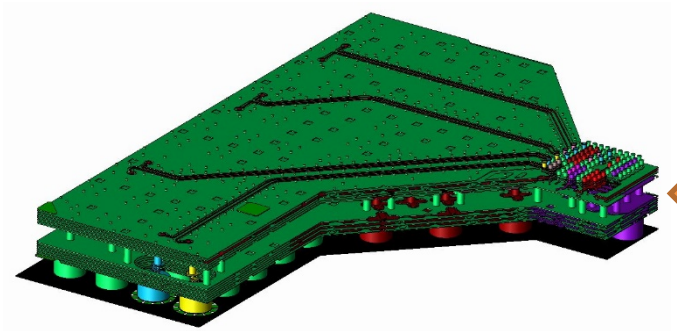
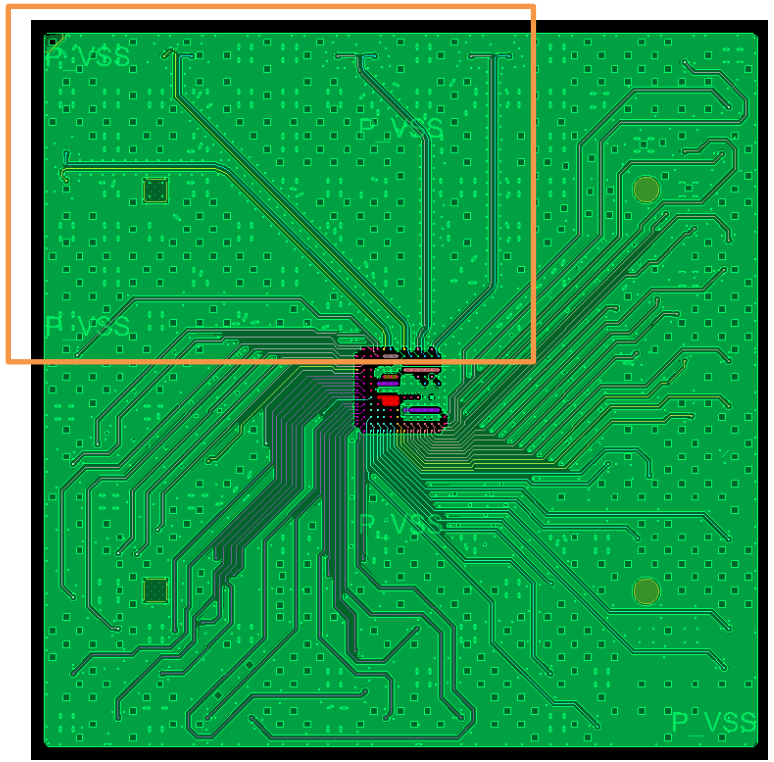
56G-PAM4 Package HSIO Design Flow

Design Flow Example: MCM Extraction of 56G PAM-4 Section of Pkg





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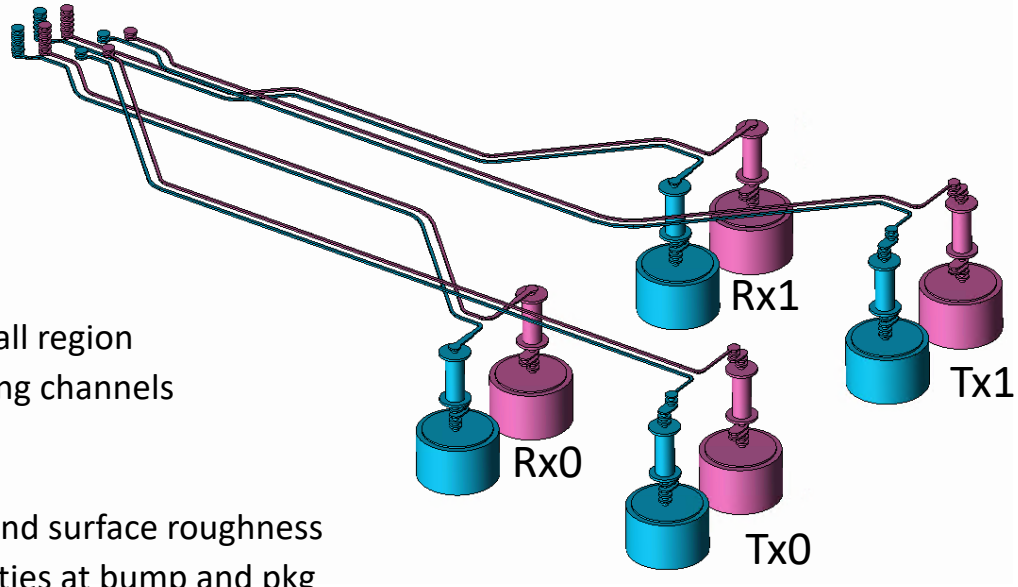
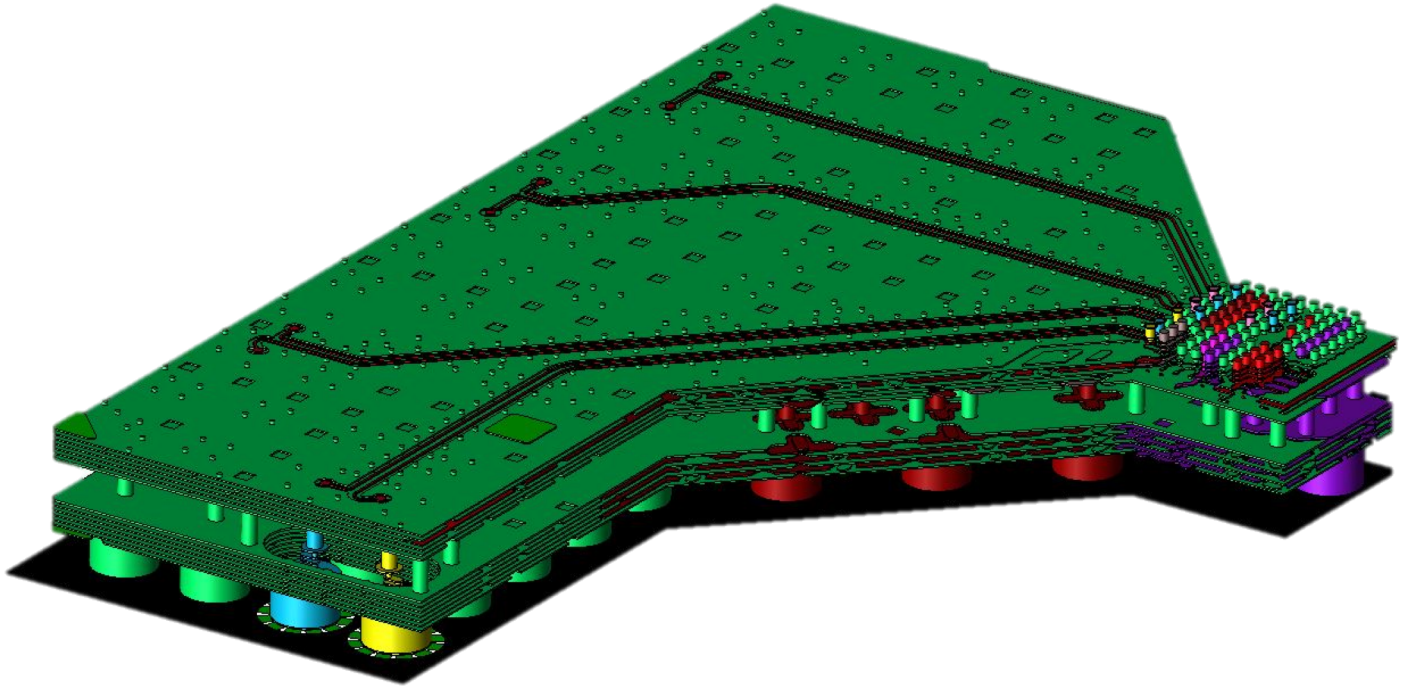
56G-PAM4 Package HSIO Design Flow

- 56G PAM-4 High speed IO (HSIO) net design primarily driven by the following impairments
  - Return losses
    - ✓ bump breakout
    - ✓ pkg ball transitions
  - Crosstalk
    - ✓ Microvia coupling in bump region
    - ✓ Transition via coupling in the pkg ball region
    - ✓ Edge-coupling along adjacent routing channels
  - Insertion Loss
    - Influenced by material properties and surface roughness
    - "Ripples" influenced by discontinuities at bump and pkg ball transitions



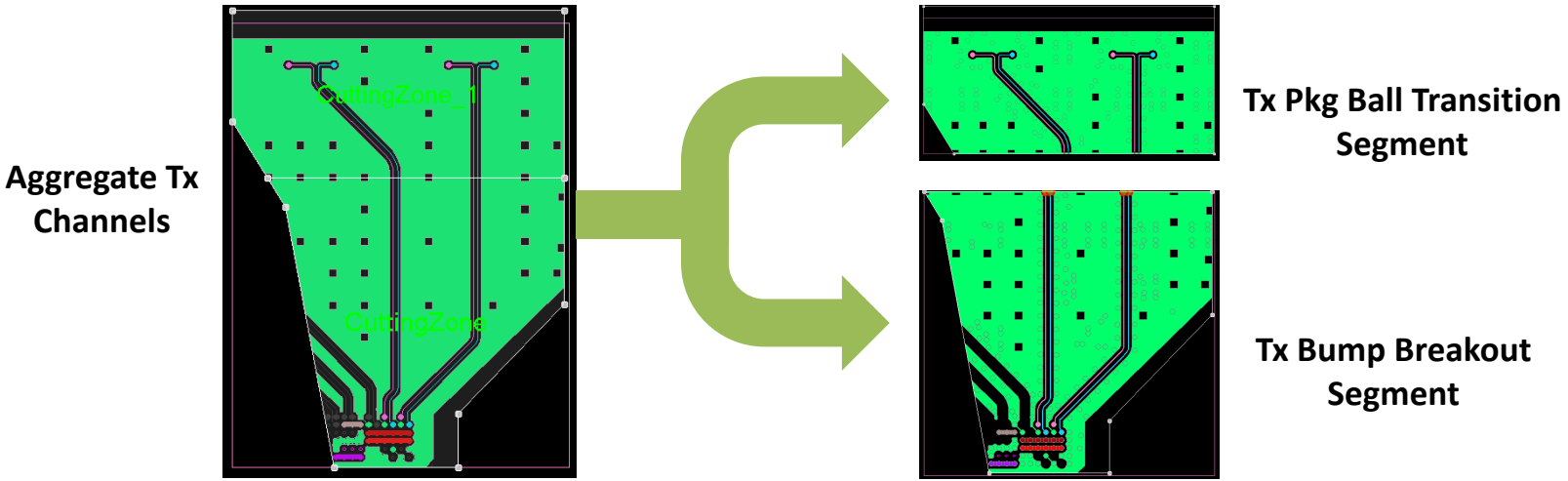
Package HSIO Design Flow

Global Package Extraction with all HSIO lanes + PLL/Ref Clks



Package HSIO Design Flow

- Traditional HSIO design flow entails segmenting the HSIO nets into localized regions to solve efficiently
  - Isolate at least 2 diff pairs in each localized region
  - Model splicing can be made efficient through “Cut-and-Stitch” flow



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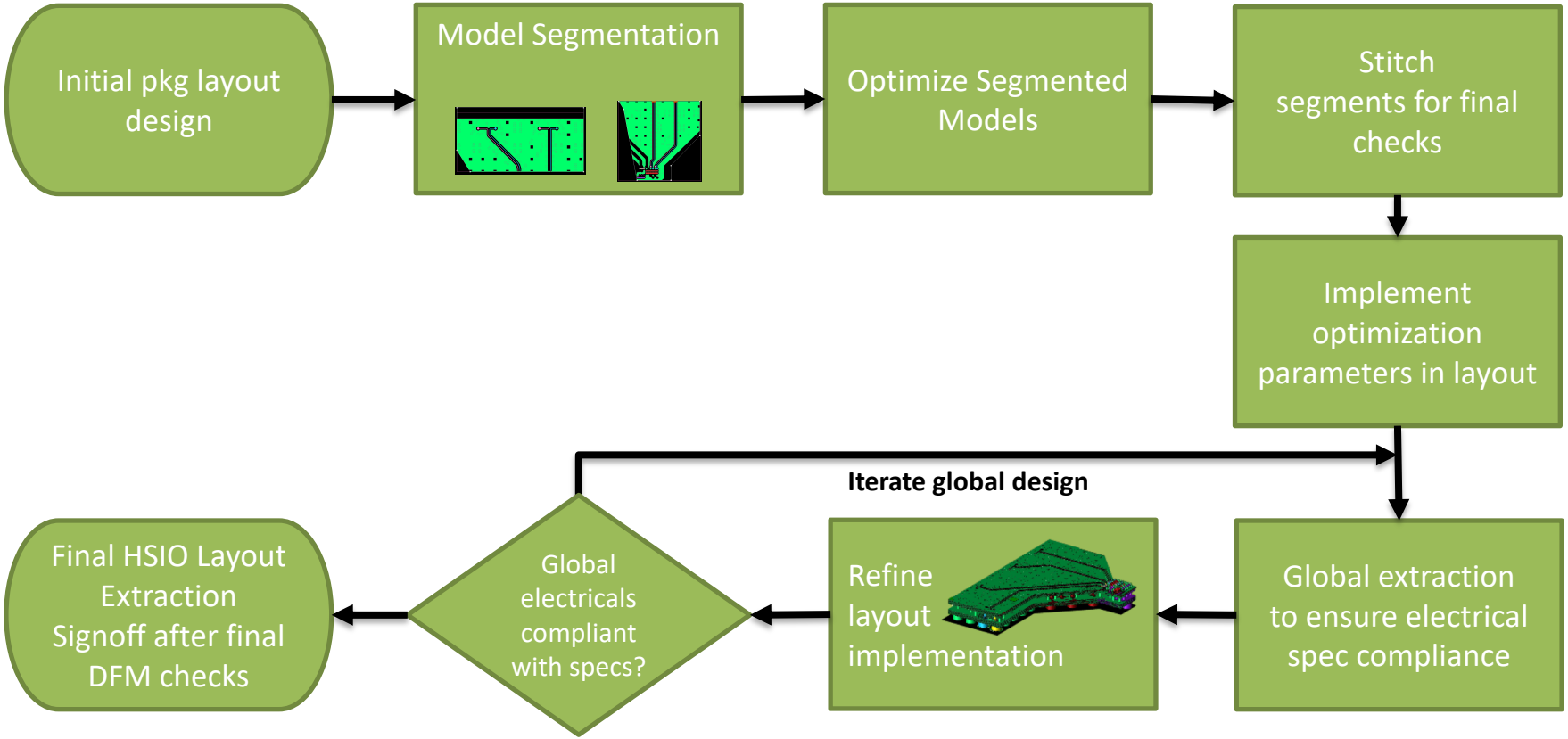


Package HSIO: Computational Flow Example

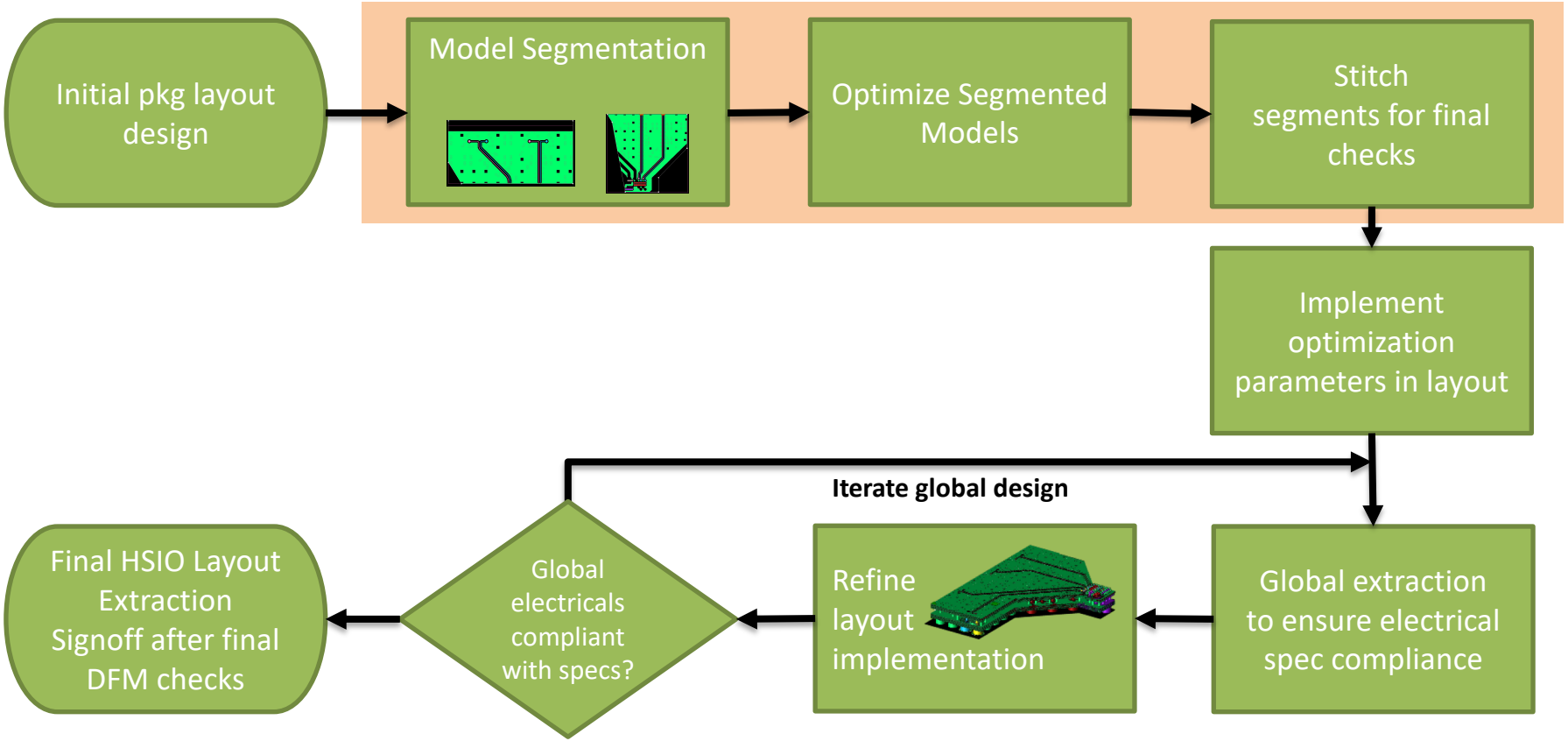
Advantages

- "Small enough" to capture XTLK between adjacent pairs
- "Small enough" to efficiently perform accurate design iterations with high resolution meshing in a single server/workstation
- Easy-to-stitch segments together to get insertion loss estimate
- Traditional methods of "brute force extractions" very time/resource consuming

Disadvantages

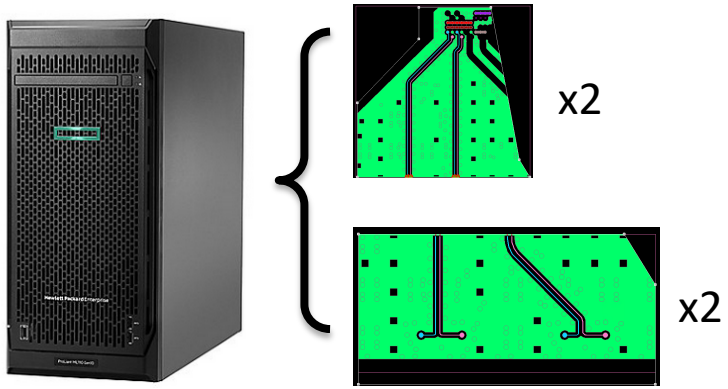
- Iterative optimizations required for each and every segment (Tx, Rx, PLL Clks, etc)
    - Remember, Tx's and Rx's are located on dedicated routing layers → transition topologies asymmetric!
- Artificial segmentation could mask certain global resonance conditions
- Still need to iterate larger aggregate model to inspect:
    - Possible secondary 3D reflections not captured by segmented model
    - Global GND/power plane resonance conditions not captured by segmented model
    - Signoff each layout iteration until final DFM checks are completed

Computational Flow Example



Discrete Segment Modeling

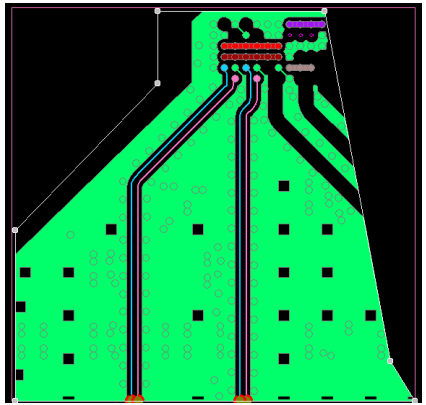
- 8-port Model segments optimizations simulated with single server tower
  - 36-core server (2.3 GHz Core Speed)
  - 1 TB total DDR4-2400 MHz RAM
  - Assume single-license utilization
- Model Permutations
  - Bump Breakout segments: 1 Tx / 1 Rx
  - Pkg Ball Transition segments: 1 Tx / 1 Rx
  - 4 total segments
- Power-SI 3D-EM General Solve Settings
  - Multi-threaded solve enabled
  - Delta |S| = 0.02 with 2 converged iterations
  - Solve frequency: 30 GHz
  - KMOR Frequency Sweep Setup
    - 10 MHz – 50 GHz
    - Sweep tolerance = 0.001
    - HPC Setup for x4 MPI's to solve 4-ports simultaneously



Tx Channel Segments: Run Times

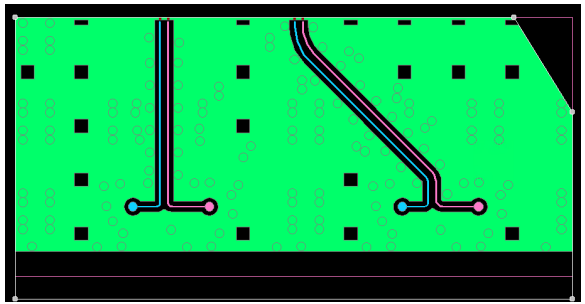
Tx Die Bump Breakout Segment

- Number of design iterations: 2
- Sim time per iteration: ~ 3 hours
- Total Sim Time: ~ 6 hours

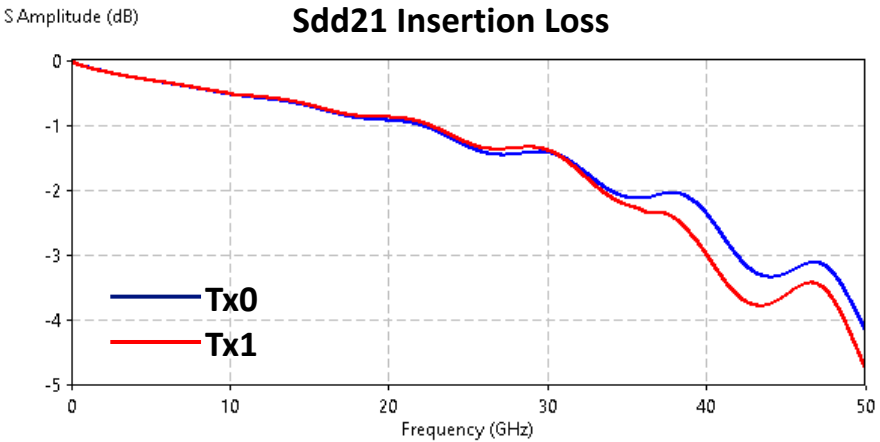


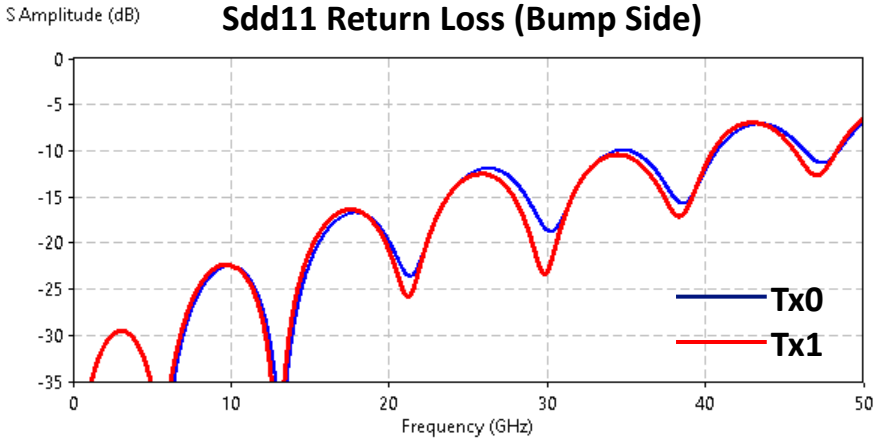
Tx Pkg Ball Transition Segment

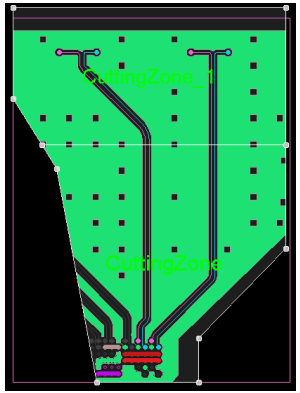
- Number of design iterations: 5
- Sim time per iteration: ~ 2 hours
- Total Sim Time: ~ 10 hours

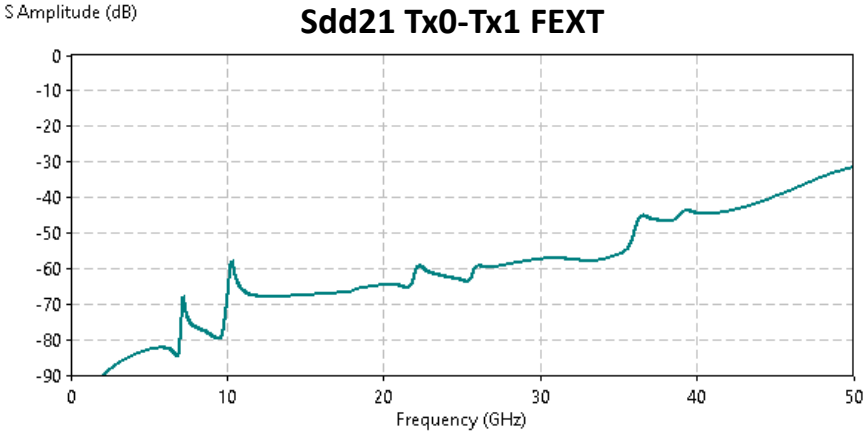


Tx Channel Segments: Stitched S-parameters









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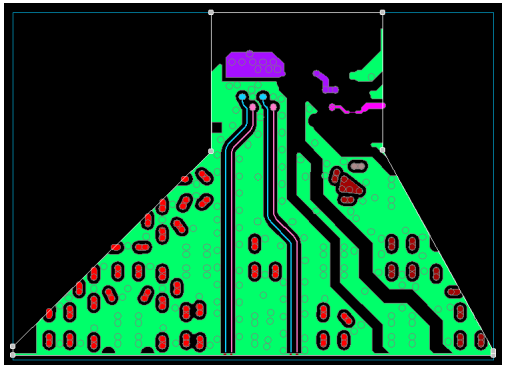
Rx Channel Segments: Run Times

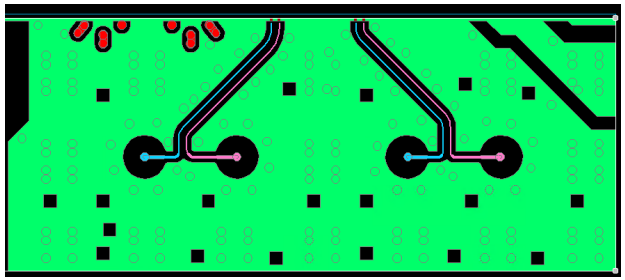
Rx Die Bump Breakout Segment

- Number of design iterations: 2
- Sim time per iteration: ~3 hours
- Total Sim Time: 6 hours

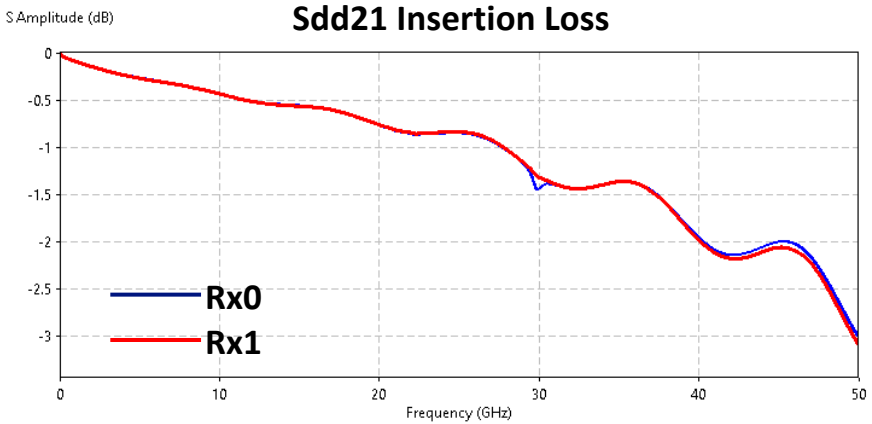


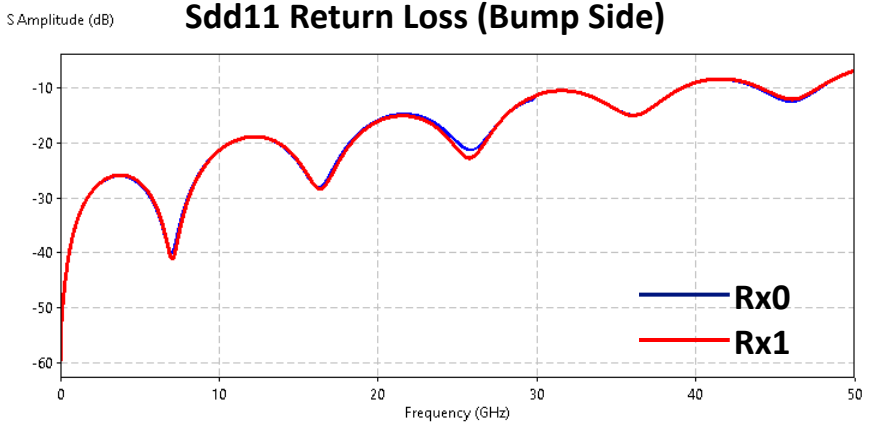
Rx Pkg Ball Transition Segment

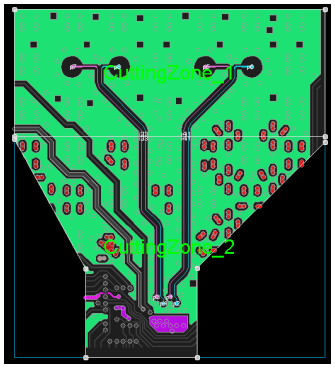
- Number of design iterations: 5
- Sim time per iteration: ~ 1.2 hours
- Total Sim Time: 6 hours

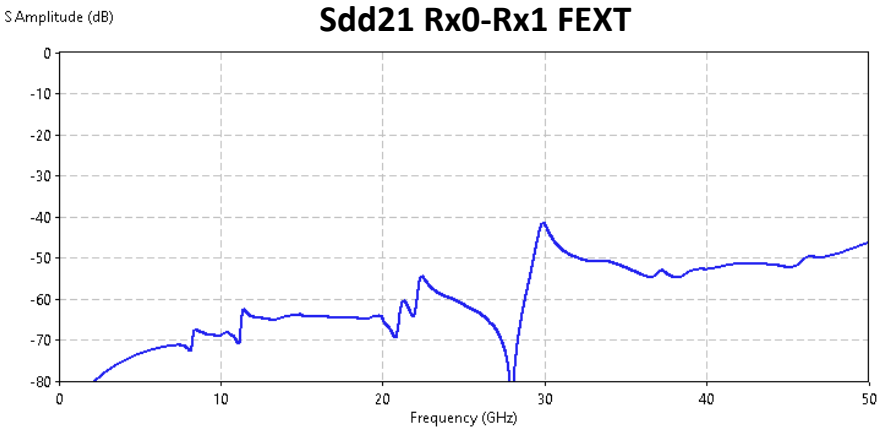


Rx Channel Segments: Stitched S-parameters









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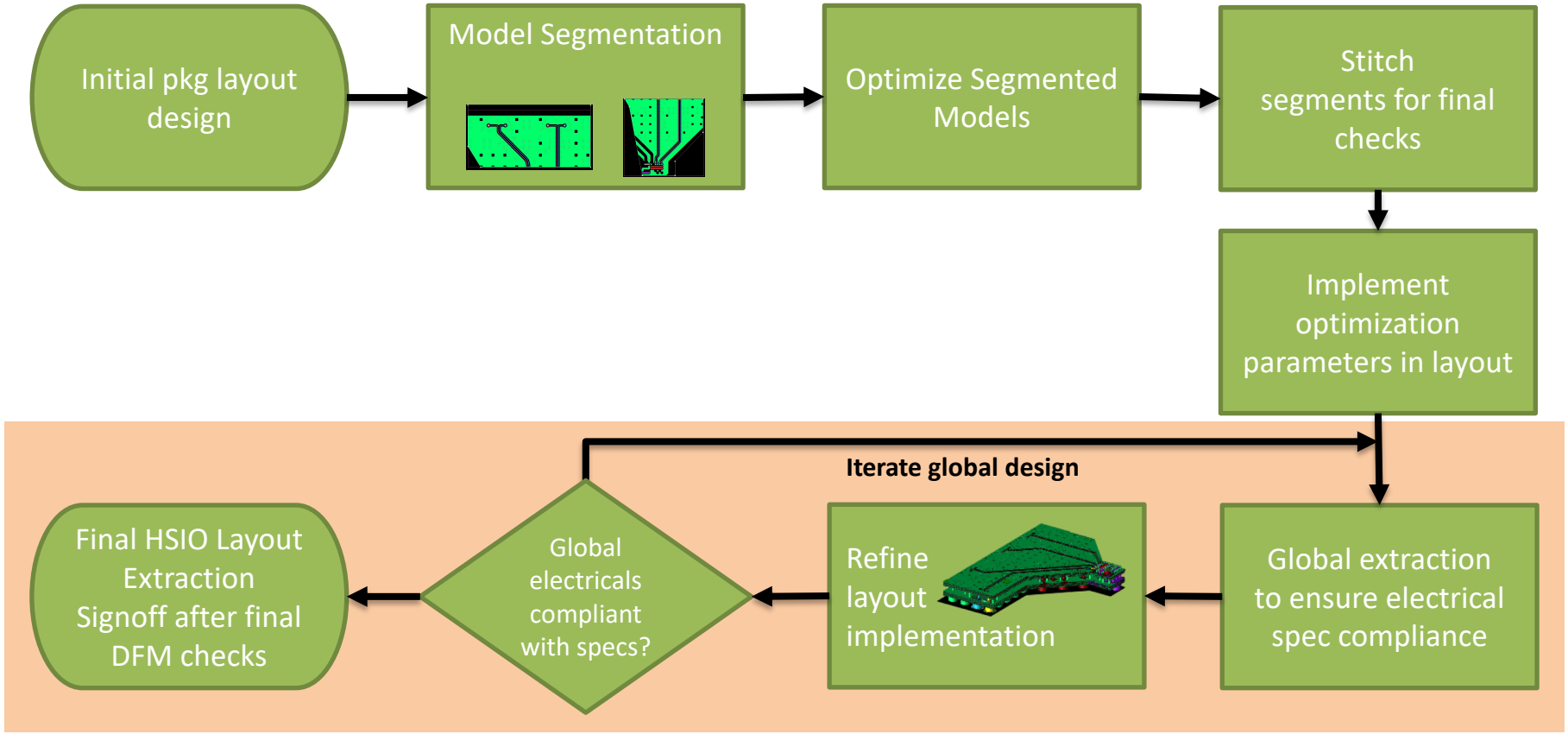
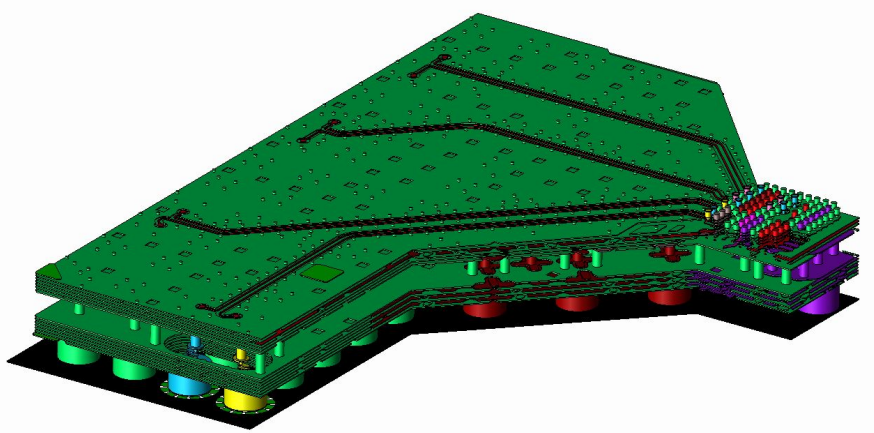
Computational Design Flow Example

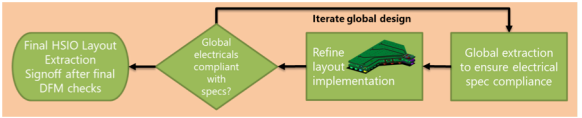


Global Model Extraction

- Global Model Extraction performed across **5 servers**
  - 180 Total CPU's / 5 TB total RAM
    - ➢ 36-cores / server (2.3 GHz Core Speed)
    - ➢ 1 TB DDR4-2400 MHz RAM / server



- Power-SI 3D-EM General Solve Settings
  - Multi-threaded solve enabled
  - Delta |S| = 0.02
  - Solve frequency: 30 GHz
  - Frequency Sweep Setup
    - ➢ 10 MHz – 50 GHz
    - ➢ Sweep tolerance = 0.001
    - ➢ HPC Setup for x15 MPI's to solve 15-ports simultaneously



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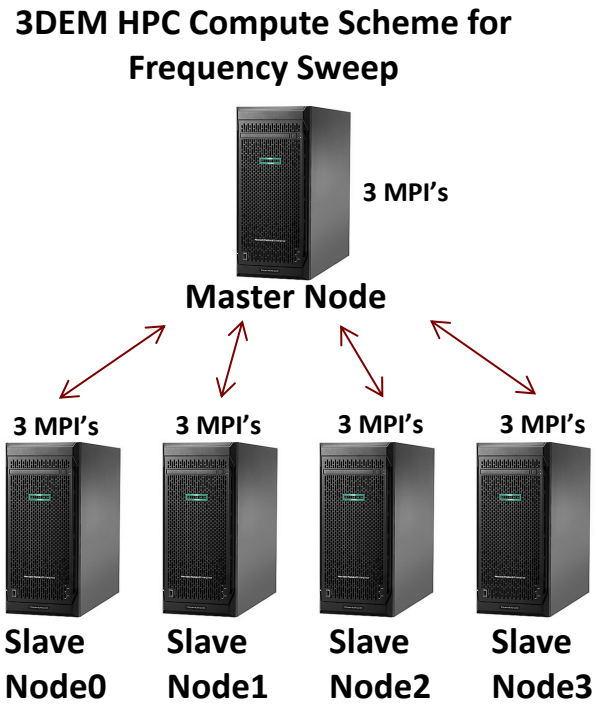
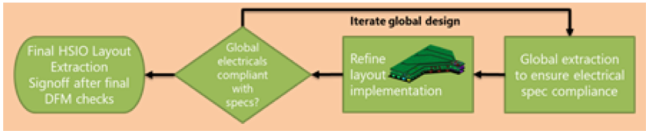
Global Model Extraction

- HPC Solve Scheme
  - Adaptive Meshing →Master node
    - ✓ Direct matrix solve with 36 cores
  - Frequency Sweeps
    - ✓ x15 MPI spread: Master + 4 slave nodes
    - ✓ 12 cpu cores / MPI

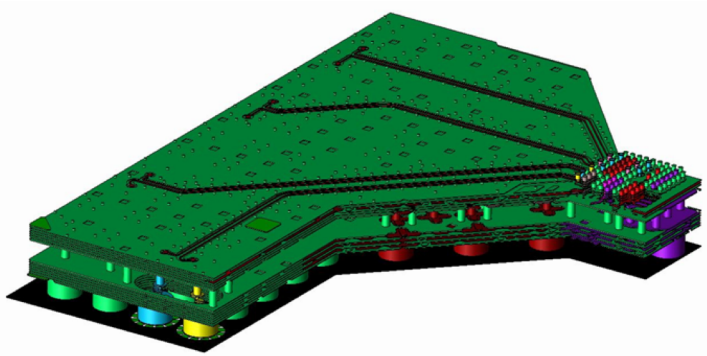


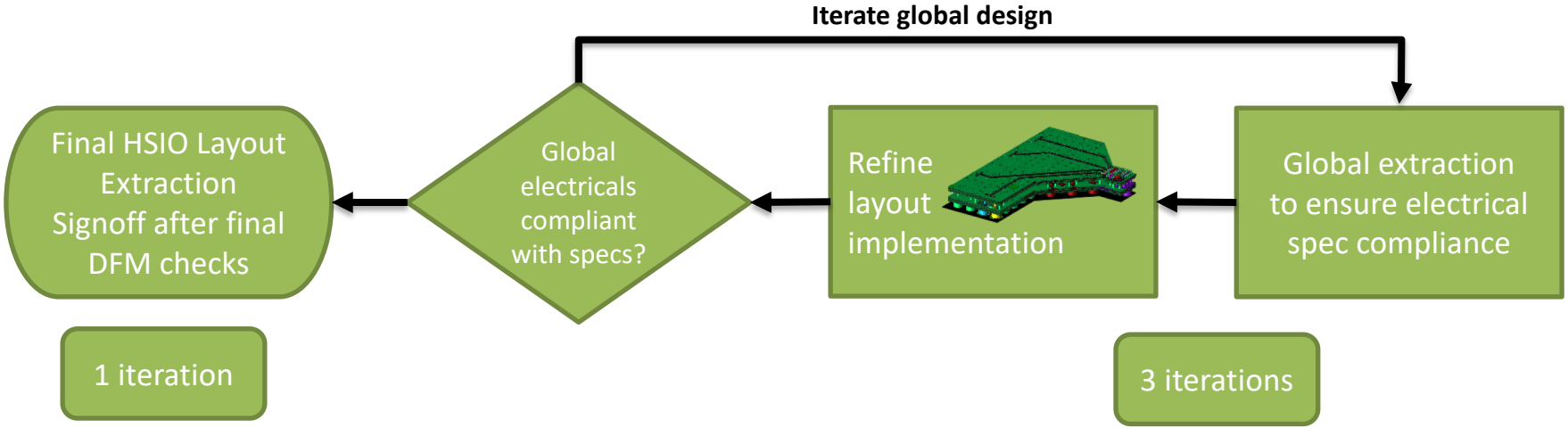


Global Model Extraction: Solve Times

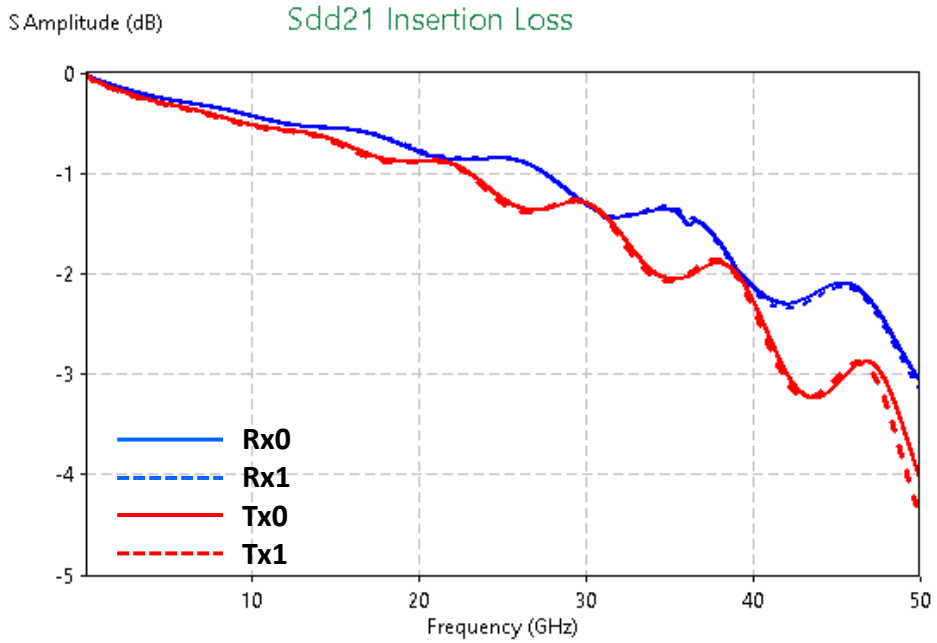
Iterative Global Extraction

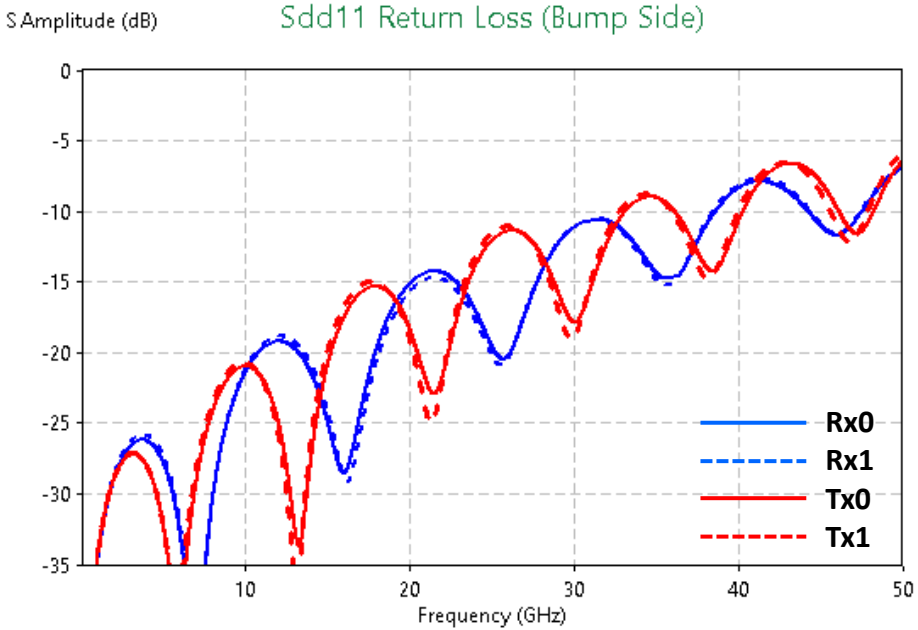
- Total solve time per Global Extraction: 15 hours
- Total # of iterations including final signoff: 4
- **Total sim time: (15x4) 60 hours**





Global Model Extraction: Final S-Parameters





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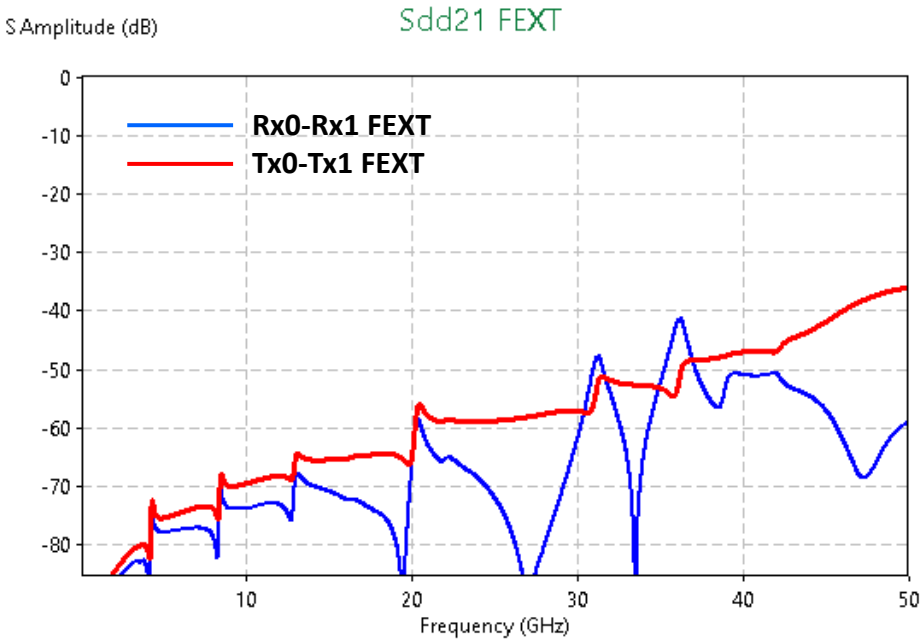
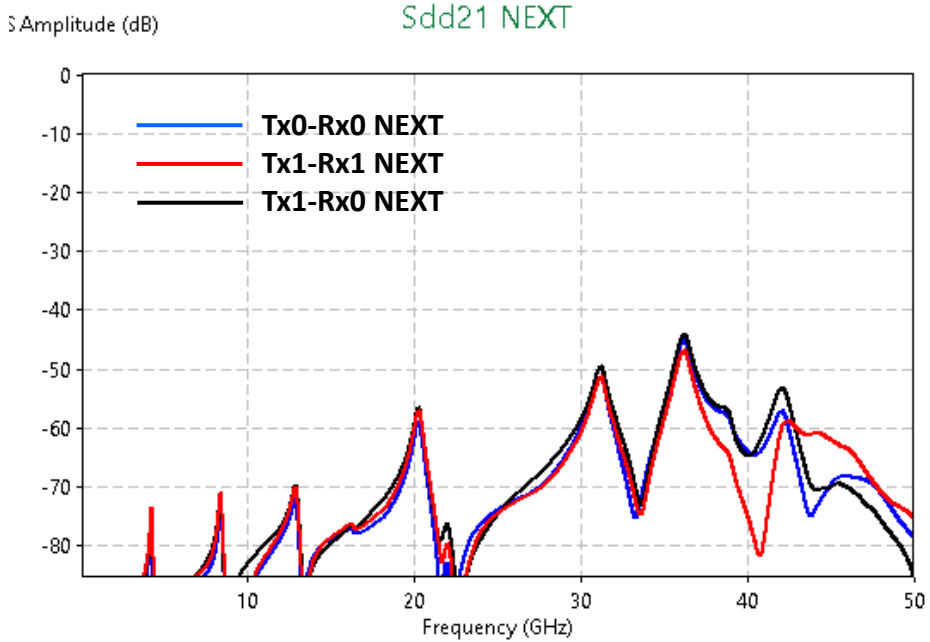
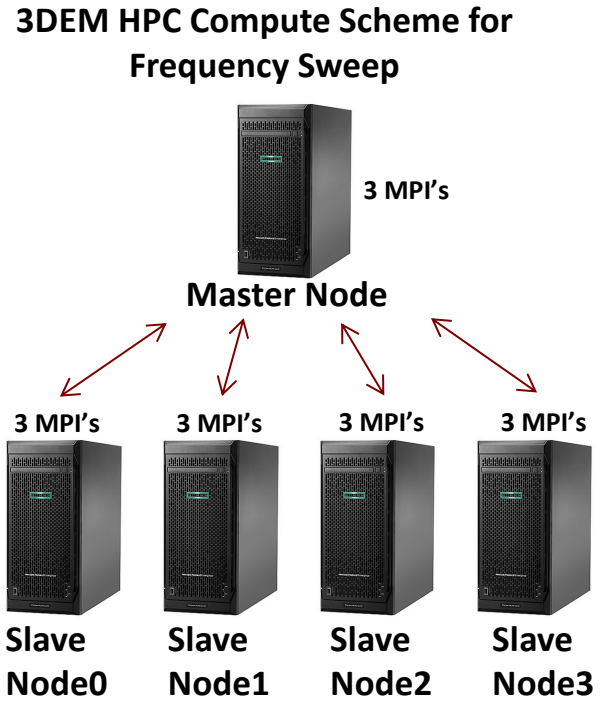




Global Model Extraction

- Solve Analytics
  - Total sim time: 15 hours / extraction
  - Peak memory consumption: 100 GB / MPI process
  - Total Peak Memory Consumption: 1.5 TB
- Solve Times
  - Model Segmentation: 28 hrs
  - Global Model Extractions: 60 hrs
  - **Total Sim Time: 88 hrs**



Package HSIO Design Flow

Bottom Line Factors

- Model segmentation flow requires lots of process steps
- Traditional FEM approach is very resource/time intensive, even with HPC
- Is there a computationally efficient, yet equally accurate method to reduce design iterations and speed-up designs?

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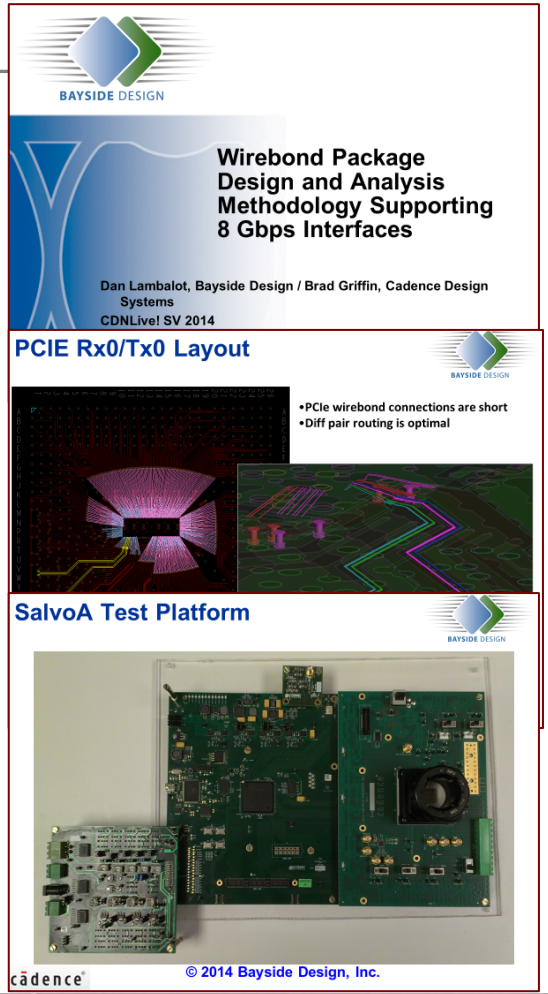
Intro to Clarity 3D Solver

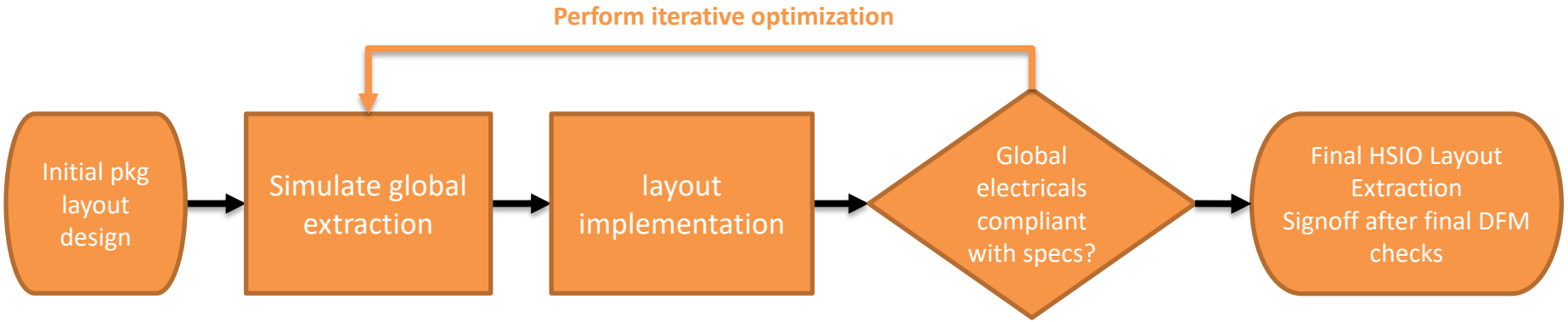
- Socionext America has access to multiple 3D analysis tools including Sigrity 3D extraction tools
  - Frequently consult on Cadence projects and emphasize use of Cadence tools when working on Cadence projects

- Feedback to Cadence has been
  - 3D analysis tools must maintain the highest accuracy
  - 3D analysis tools require too much memory
  - 3D tools need to be scalable across multiple cores / machines (optionally available to run in the cloud)
  - 3D tools should not crash when memory resources are stretched

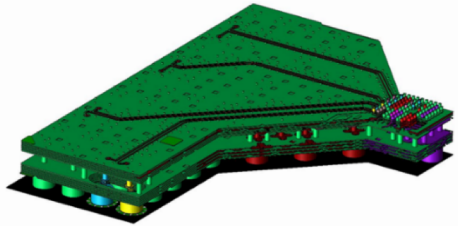
- Cadence has now introduced us to Clarity 3D Solver
  - They have been listening!
  - Yes, there is there a computationally efficient, yet equally accurate method to reduce design iterations and speed-up designs!



Accelerated Computational Prototyping Flow: Clarity 3D Solver



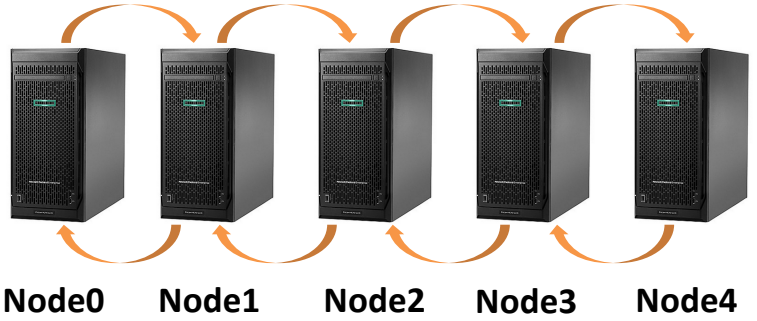
- Accelerated field solver times permits prototyping of enlarged extractions
- Simultaneously optimize all sources of HSIO impairments with each iteration
  - No need to iterate smaller segments
  - Eliminates need for global extractions to validate stitched segments and to compensate for additional impairments that segmentation approach does not capture (e.g. GND resonance)



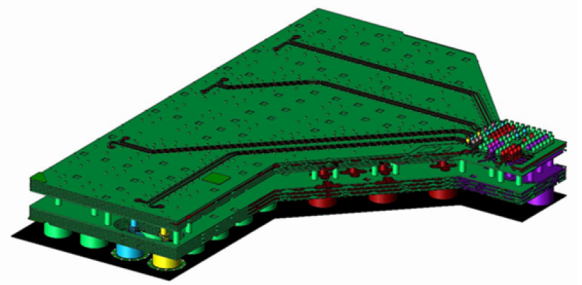
Accelerated Computational Prototyping Flow: Clarity 3D Solver

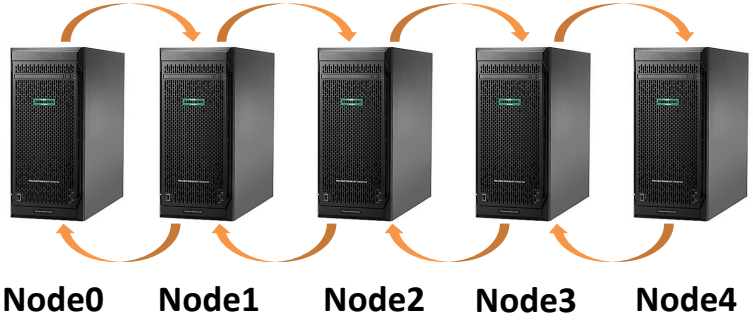
- Global Model Extraction across **5 servers**
  - 180 Total CPU's / 5 TB total RAM
    - 36-cores / server (2.3 GHz Core Speed)
    - 1 TB DDR4-2400 MHz RAM / server

- Clarity Solve Settings
  - True parallelized matrix computation flow with all resources
  - Delta |S| = 0.02 with 2 converged iterations
  - Solve frequency: 30 GHz
  - Frequency Sweep Setup
    - 10 MHz – 50 GHz
    - Sweep tolerance = 0.001



Accelerated Computational Prototyping Flow: Clarity 3D Solver



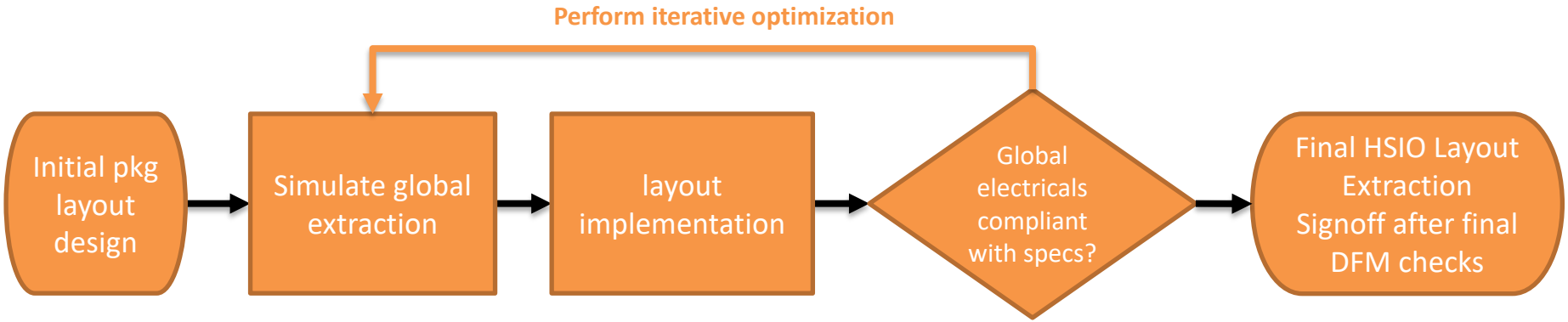


Solve Analytics

Total sim time: **2 hours / Global Extraction** → **7.5x Faster than 3DEM with HPC**

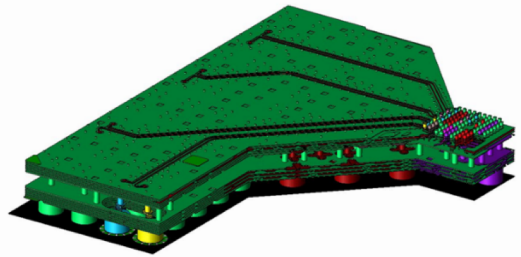
Total Peak Memory: 170 GB → **8.8x less memory than 3DEM with HPC**

Accelerated Computational Prototyping Flow: Clarity 3D Solver



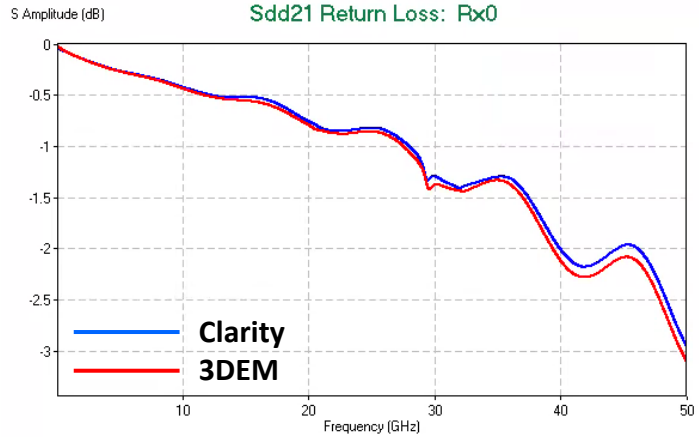
Iterative Global Extractions

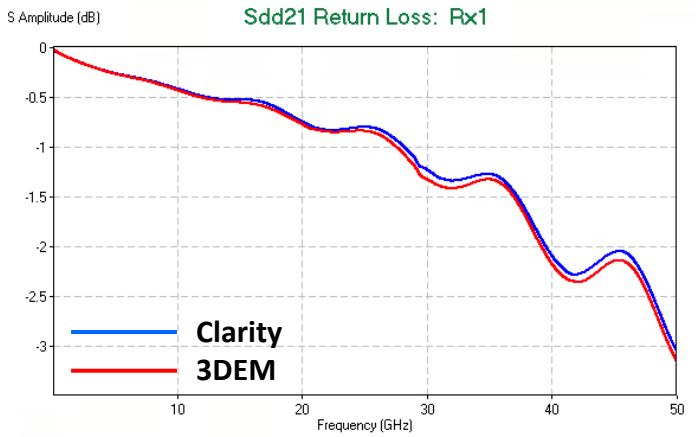
- Extraction Cycles
  - Design iterations: 5 (governed by package ball transition region since this requires the most number of iterations)
  - Final signoff: 1
- **Total sim time: (2x6) = 12 hours**

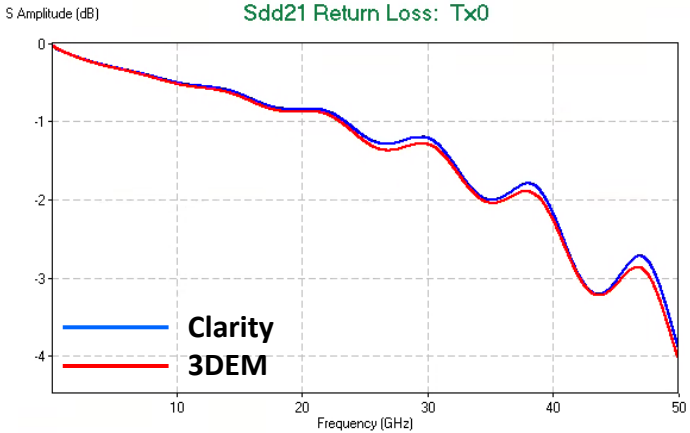


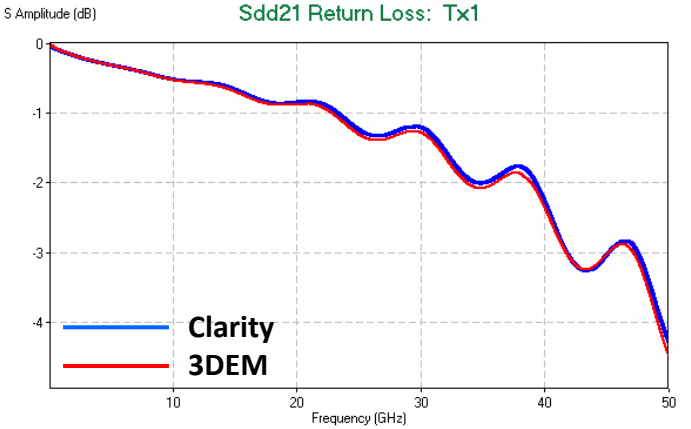
Global Model Extraction: Final S-Parameters

Global Model Extraction: Final S-Parameters

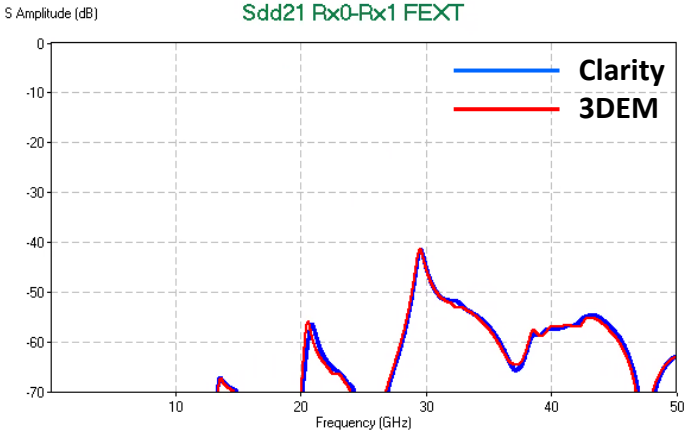


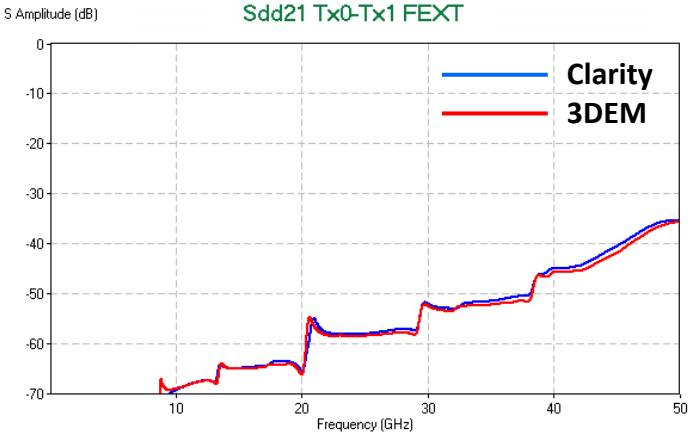


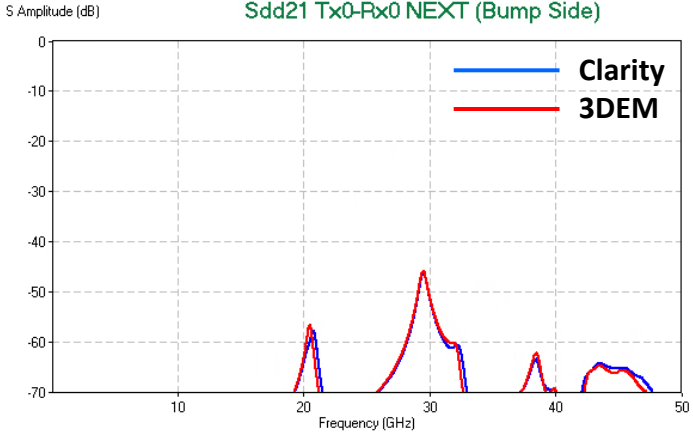


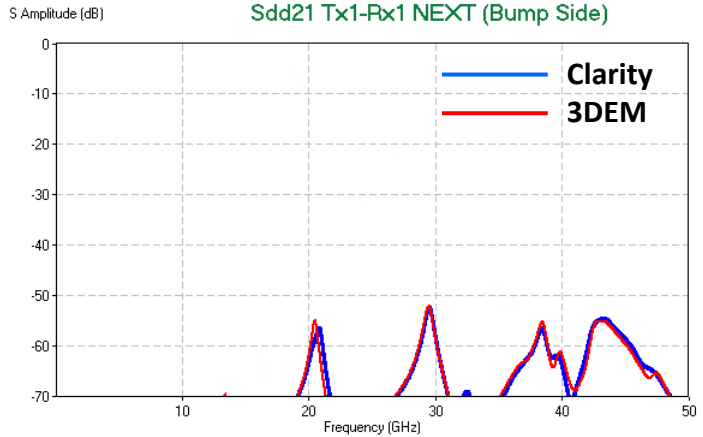


Global Model Extraction: Final S-Parameters









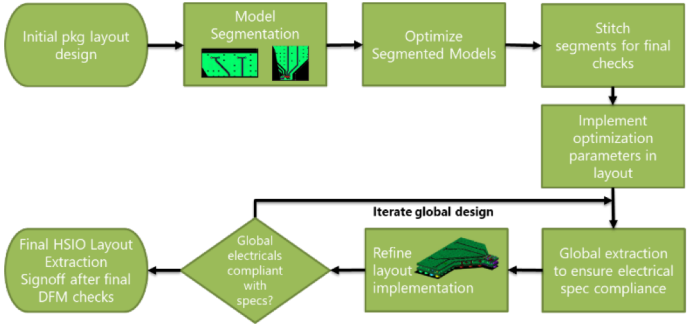
Agenda

- Intro to Socionext America
- Review Test Case
- Pros & Cons of Traditional High-Speed IO Modeling Flow using Model Segmentation Approach
  - Computational Design Flow
- Introduction to Clarity 3D Solver
- Streamlined Approach: No Model Segmentation Necessary
  - Accelerated Computational Prototyping Flow
- Comparison of Approaches

Comparison: Traditional Flow vs. Clarity 3D Solver Flow

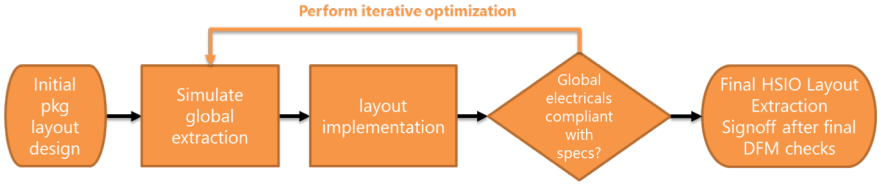
Traditional 3D Expert Flow

- Segmentation Required



Clarity 3D Solver Flow

- **No** Segmentation Required
- **Accelerates** HSIO Package Design by **7.3x**



	3D-EM Traditional Segmentation Flow	Clarity Accelerated Prototyping Flow
Model Segment Optimization	28 Hours	-
Global Model Extractions/ Optimizations	60 Hours	12 Hours
Total Sim Design Time	**88 Hours**	**12 Hours**

Conclusions

- Cadence Clarity 3D Solver addresses the primary challenges with 3D modeling
  - Accuracy
  - Speed
  - Capacity
  - Cost of computing resources

- Accelerated 3D model extraction times with correlated accuracy
  - Increased flexibility to iterate/improve package designs
  - Enables meeting project milestones and consistently serving our customers in a timely manner

socionext™

for better quality of experience